PATENT APPLICATION
DOCKET NO.: 10012773-1

LISTING OF THE CLAIMS PER 37 C.F.R. §1.121

1. (Original) A SYNC pulse compensation apparatus, comprising:

a sampling compensation circuit operable to condition a SYNC pulse signal, wherein said SYNC pulse signal is based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion; and

a jitter cycle delay compensation circuit coupled to said sampling compensation circuit, said jitter cycle delay compensation circuit operating to tap said SYNC pulse signal after a predetermined delay based on a skew difference between said first and second clock signals.

2. (Original) The SYNC pulse compensation apparatus as set forth in claim 1, wherein said sampling compensation circuit comprises a plurality of multiplexers arranged in series, each multiplexer operating to receive an input through a timing register associated therewith.

3. (Original) The SYNC pulse compensation apparatus as set forth in claim 2, wherein said multiplexers are operable to insert a logic high condition in said SYNC pulse signal when said SYNC pulse signal is sampled to contain a plurality of logic lows during a predetermined time window.

4. (Original) The SYNC pulse compensation apparatus as set forth in claim 2, wherein said plurality of multiplexers comprises three multiplexers operable to insert a [010] sequence in said SYNC pulse signal when said SYNC pulse signal is sampled to be all zeros during a predetermined time window.

5. (Original) The SYNC pulse compensation apparatus as set forth in claim 1, wherein said jitter cycle delay compensation circuit comprises:

a series of delay registers, each operating to delay said SYNC pulse signal by a predetermined amount of time; and

a multiplexer operable to select a delayed SYNC pulse output generated from said series of delay registers.

6. (Original) The SYNC pulse compensation apparatus as set forth in claim 5, wherein said series of delay registers comprises eight registers.

7. (Original) The SYNC pulse compensation apparatus as set forth in claim 5, wherein said multiplexer is actuated by a JITTER-STATE control signal generated by a state/correct block responsive to said skew difference between said first and second clock signals.

8. (Original) The SYNC pulse compensation apparatus as set forth in claim 7, wherein said state/correct block is coupled to a phase detector operating to detect said skew difference between said first and second clock signals.

9. (Original) The SYNC pulse compensation apparatus as set forth in claim 7, wherein said JITTER-STATE control signal is stored in a flip-flop.

10. (Currently Amended) A SYNC pulse compensation method, comprising:

sampling a SYNC pulse signal generated based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion; and

if said SYNC pulse signal is sampled to contain an anomalous condition during a predetermined time period, removing said anomalous condition by activating appropriate SYNC correct control logic ~~a plurality of logic lows during a predetermined time period, inserting a logic high condition at a select point in time~~.

11. (Original) The SYNC pulse compensation method as set forth in claim 10, wherein said second clock signal is generated by a phase-locked loop (PLL) based on said first clock signal.

12. (Original) The SYNC pulse compensation method as set forth in claim 10, wherein said SYNC pulse signal is generated when a rising edge in said first clock signal coincides with a rising edge in said second clock signal.

13. (Previously Presented) The SYNC pulse compensation method as set forth in claim 12, further comprising, if said SYNC pulse signal is sampled to indicate a duplicate logic high condition during a predetermined time period, masking said duplicate logic high condition.

14. (Previously Presented) A SYNC pulse compensation method, comprising:

sampling a SYNC pulse signal generated based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion;

determining a clock state indicative of a phase difference between said first and second clock signals;

re-positioning said SYNC pulse signal based on said clock state; and

if said SYNC pulse signal is out-of-phase by a predetermined amount with respect to said first clock signal, delaying said SYNC pulse signal based on said clock state.

15. (Original) The SYNC pulse compensation method as set forth in claim 14, wherein said SYNC pulse signal is re-positioned by adding at least an extra clock cycle when said clock state indicates that said first clock signal lags with respect to said second clock signal by a predetermined amount.

16. (Original) The SYNC pulse compensation method as set forth in claim 14, wherein said SYNC pulse signal is re-positioned by deleting at least an extra clock cycle when said clock state indicates that said second clock signal lags with respect to said first clock signal by a predetermined amount.

17. (Original) The SYNC pulse compensation method as set forth in claim 14, wherein said SYNC pulse signal is delayed by propagating said SYNC pulse signal through a series of delay registers operable to be selected by a multiplexer in response to a JITTER-STATE control signal corresponding to said clock state.

18. (Original) The SYNC pulse compensation method as set forth in claim 17, wherein said JITTER-STATE control signal is stored in at least one flip-flop.

19. (Original) The SYNC pulse compensation method as set forth in claim 14, wherein said first and second clock signals comprise a core clock and a bus clock, respectively, in a computer system.

20. (New) A SYNC pulse compensation method, comprising:

sampling a SYNC pulse signal generated based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion, wherein said SYNC pulse signal is generated when a rising edge in said first clock signal coincides with a rising edge in said second clock signal; and

if said SYNC pulse signal is sampled to indicate a duplicate logic high condition during a predetermined time period, masking said duplicate logic high condition.